A SINUSOIDAL PWM SCHEME FOR NEUTRAL POINT CLAMPED FIVE LEVEL INVERTER

SRIHARIRAO NAMBALLA
Power Electronics, Department of Electrical & Electrical Engineering,
Visakha institute of Engg& Tech, Visakhapatnam,(A.P), India.
E-mail: srihari63@gmail.com

Abstract: A power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. Some advantages that multilevel inverters have compared to two level inverters are minimum harmonic distortion, reduced EMI/RFI generation, and operation on several voltage levels. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and a machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, the fact that they are a lot harder to build, they are more expensive, and they are more difficult to control in software. This focus of the simulation is on study of three phase, three-level, and five-level inverters. Full analysis for three-level and five-level inverter is included .Software packages MATLAB/SIMULINK is used to study and simulate inverter waveforms. Firstly, three phase inverters are modeled with resistive load and inductive load and their waveforms are observed. Secondly, a three-level inverter is modeled by different ways and suitable switching control strategies (PWM technique) to carry out harmonic elimination. Thirdly, a five-level inverter is modeled by different ways and suitable switching control strategies (PWM technique) to carry out harmonic elimination. Finally, all inverters models are modeled and run in by using MATLAB/SIMULINK. Three level and five level inverters both three-phase are modeled, run and compared.

Index Terms—Multilevel inverter, neutral point clamped (NPC), sine pulse width modulation (SPWM), switching state, five-level inverter

1. Introduction:
The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, they are more expensive, and they are more difficult to control in software. This paper focuses on the analysis of a three-level inverter of desirable voltage and frequency has been achieved; however, harmonics distortion should be investigated during operation. The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. Even though sine pulse width modulation (SPWM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. Different aspects of the three-level NPC inverter will be discussed including the inverter topology. The operation theory will be discussed with the aspect of sine pulse width modulation.

2. Five-level NPC inverter:
Multilevel topologies and modulation techniques have been developed and applied in high power systems. With the requirement of quality and efficiency in high power systems with the limitation of high power device switching speed, low total harmonic distortion (THD) and low switching frequency are desirable. MULTILEVEL conversion structures represent a solution to improve the performances given by the classical structures with two voltage levels. Multilevel structures offer a reduction of the voltage stress that compensates the increased number of devices. Also these structures offer the advantage of reducing the size of the output filter by reducing the total harmonic content.

An important structure is the Active Neutral Point Clamped Converter (ANPC) developed in 2001. It presents the advantage of an increased number of degrees of freedom. Also it allows the combination with other concepts in order to create structures with higher number of voltage levels and output parameters. Another class of multilevel converters introduces the coupled inductor concept. This type of converters offers an increased number of voltage levels, lower current stress in the semiconductor devices and better output voltage properties.

The most commonly used topologies are neutral-point-clamped (NPC). In neutral-point-clamped inverter the dc-link is split into number of smaller voltage levels using a bank of series connected bulk capacitors. The inverter structure allows the connections of the inverter poles to any of these voltage levels, thus generating a multi-level voltage waveform at the output.

A three-phase five-level diode-clamped inverter is shown in Figure 1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by four capacitors into six levels. The voltage across each capacitor is \( V_{dc} \) and the voltage stress across each switching device is limited to \( V_{dc} \) through the clamping diodes. Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage \( V_0 \) as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg a are \((S_{a1}, S_{a'1}), (S_{a2}, S_{a'2}), (S_{a3}, S_{a'3})\) and \((S_{a4}, S_{a'4})\). Table also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series.

<table>
<thead>
<tr>
<th>Voltage Vao</th>
<th>Switching state</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( S_{a4} )</td>
</tr>
<tr>
<td>( V_4 = 4V_{dc} )</td>
<td>1</td>
</tr>
<tr>
<td>( V_3 = 3V_{dc} )</td>
<td>0</td>
</tr>
<tr>
<td>( V_2 = 2V_{dc} )</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig. 1. Three-phase five-level structure of a neutral point clamped inverter.
The advantages of NPC inverter are:
(i) All of the phases share a common dc bus, which minimizes the capacitance requirements of the inverter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
(ii) The capacitors can be precharged as a group.
(iii) Efficiency is high for fundamental frequency switching.

3. Sinusoidal pulse width modulation (SPWM): In sinusoidal PWM instead of maintaining the width of all pulses the same as in the case of multiple PWM, the width of each is varied in proportion to the amplitude of a sine wave evaluated at the same pulse. The distortion is reduced significantly compared to multiple PWM (Figure 2).

### Table 1: Output voltage levels with switching states

<table>
<thead>
<tr>
<th>$V_1 = 1V_{dc}$</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_0 = 0$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Fig 2. Spwm generating gate pulses

A high frequency triangular wave, called the carrier wave, is compared to a sinusoidal signal representing the desired output, called the reference wave. Usually, ordinary signal generators produce these signals. Whenever
The carrier wave is less than the reference, a comparator produces a high output signal, which turns the upper transistor in one leg of the inverter on the lower switch off. In the other case the comparator sets the firing signal low, which turns the lower switch ON and upper switch OFF.

The number of pulses per half cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm cannot conduct at same time, the instantaneous output voltage can be generated by using unidirectional triangular carrier wave as in Figure-5 this method is preferable and easier to implement. The output voltage can be varied by varying the modulation index ‘m’. The area of each pulse corresponds approximately to the area under the sine wave between the adjacent mid points of off-periods on the gating signals. The SPWM, which is most commonly used, suffers from certain drawbacks like low fundamental output voltage.

Advantages of SPWM:

- The output voltage control is easier with PWM than other schemes and can be achieved without any additional components.
- The lower order harmonics are either minimized or eliminated altogether.
- The filtering requirements are minimized as lower order harmonics are eliminated and higher order harmonics are filtered easily.
- It has very low power consumption.
- The entire control circuit can be digitized which reduces the susceptibility of the circuit to interference.

Sinusoidal Pulse Width Modulation (SPWM) technique is used to generate the gate pulses. SPWM technique is widely used in industries. Neutral point clamped Three Level Inverter is the modified version of Three Level Inverter also discussed in this paper. FFT is used for harmonic analysis of output of Three Level Inverter. Simple Block Diagram of whole system is given in Fig.3

4. Simulation results: Simulation of various inverters using sinusoidal pulse width modulation was carried out with the help of “MATLAB 6.5”. Simulation was carried out to observe the improvement in the line voltage THD and Line Current THD as the inverter level increases from 3-level and 5-level. The fig.4 and fig.5 shows final simulation diagram and corresponding simulation results of line voltages and THD results are shown in fig.6, fig.7 and also fig. 8 shows THD analysis of 3-level inverter.
A SINUSOIDAL PWM SCHEME FOR NEUTRAL POINT CLAMPED FIVE LEVEL INVERTER
5. Performance Comparison Of Three & Five Level Inverters:

As we know that the output obtained from a three-level inverter is not a pure sinusoidal waveform. It is due to the presence of harmonics in the inverter output voltage which may cause heavy losses and may lead to low efficiency or any other applications which may take the supply from the inverter. So, there is a need for us to reduce these harmonics. The harmonics in a three level inverter is reduced by increasing the switching frequency. But the switching frequency is restricted by the switching losses in high power applications. In such applications multilevel inverters have been widely used in recent years for the advantage of low harmonic output at low switching frequency. At the same time low blocking in the switching devices can be achieved. The more the number of levels of the output voltage the lesser will be the harmonic content. Multi level inverters have advantages of good power quality, good electromagnetic compatibility, low switching losses, high voltage capability. These multi level inverters are used in the active rectifiers and the FACTS applications. The multi level inverters synthesize several voltage levels from the various levels of the DC input. A near sinusoidal voltage waveform can be generated.
International Electrical Engineering Journal (IEEJ)
ISSN 2078-2365

from the various levels of the DC input. They have become attractive in the high power and high voltage applications. By using the multilevel inverters the stress on each device is reduced proportional to the number of the output levels present. With several levels in the output waveform the switching $dv/dt$ stresses are reduced, and hence the lifetime of motor and cables are increased. By using a multilevel inverter the power rating of the equipment can enhanced without any dangerous consequences.

From the simulation results, I can say that the total harmonic distortion reduces by increasing the number of levels in the output voltage and by the sinusoidal pulse width modulation technique the total harmonic distortion reduces. From the waveforms obtained I can say that the output peak voltage also increases with SPWM technique. The switching losses also reduce with the SPWM technique.

The THD for the three-level SPWM is obtained as 42.50% and five-level SPWM are obtained as 27.95% shown in fig8&7 respectively. It can be observed that the control strategy has operated at a satisfactory level.

6.Conclusions:
The following conclusions have been made on five level NPC inverter. A number of issues were investigated, including the inverter configuration, operating principle, sinusoidal modulation (SM) techniques, and neutral point voltage control. The performance of the three-phase five-level twenty four switch inverter has been explained and observed that performance of the inverter is improved by employing SPWM control scheme. Sinusoidal pulse width modulation algorithm has been described and applied to three-level, five-level inverter. Compared with conventional methods, this method has the advantage of ease implementing, especially for the inverters with more levels. From simulation results it is observed that the generated voltage spectrum is very much improved with increase the level of inverter. The use of five-level inverters reduces the harmonic components of the output voltage compared with the three-level inverter at the same switching frequency. The total harmonic distortion (THD) is highly reduced as the level of the inverter is increases. So no need additional reactors or transformers to reduce the harmonic components. Then, it is suitable for high voltage and high power applications.

7.References:
[8] Jun Hu and Jie Chang, Rockwell Science Center, 1049 Camino Dos Rios Thousand

[9] Hind Djeghloud, Hocine Benalla, Space Vector Pulse Width Modulation Applied to the Three-Level Voltage Inverter, Electrotechnic's Laboratory of Constantine, Mentouri-Constantine University, Constantine 25000, Algeria.

[10] Ayşe Kocalmuş and Sedat Sünter, Simulation of a Space Vector PWM Controller for a Three-Level Voltage-Fed Inverter Motor Drive, Department of Electrical and Electronic Engineering, Fırat University, 23119, Elazığ.